Full Wave Analysis of Planar Interconnect Structures Using FDTD–SPICE

N. Orhanovic, R. Raghuram, and N. Matsui
Applied Simulation Technology
1641 N. First Street, Suite 170
San Jose, CA 95112
{neven, raghu, matsui}@apsimtech.com

Abstract
This paper describes a full wave approach for analyzing planar interconnect structures, such as power distribution systems in printed circuit boards and multichip modules, using a tightly coupled combination of FDTD and SPICE. The technique enhances the present hybrid full wave circuit methods in terms of robustness and efficiency. The method is applied to a few sample problems to illustrate its accuracy and versatility.

1. Introduction
Accurate analysis of planar interconnect structures, such as printed circuit boards (PCBs) and multi chip modules, is critical for the efficient design of GHz systems. Problems such as power distribution system design, determining the locations and the number of decoupling capacitors, and noise containment require complex modeling and a significant amount of computational effort. The treatment of general nonlinear circuit elements complicates the analysis further.

These problems are often dealt with by producing various quasi-static circuit models or frequency domain mathematical macromodels of the linear interconnect structure (e.g., [1]–[3]). While these models can be simple to use, they are still difficult and computationally costly to produce and often do not give the required accuracy in the time domain. This is especially true if full wave accuracy is needed.

An attractive alternative to frequency domain modeling is to extend the widely used finite difference time domain (FDTD) method to include lumped circuit elements. For simple linear elements the lumped element equations can be handled directly in FDTD. For more general elements they must be handled by a general circuit simulator such as SPICE. The quasi-static assumption made at the ports where the circuit elements are connected holds as long as the port dimensions are much smaller than the shortest wavelength of the signals propagating in the structure. This is true for a wide variety of analog and digital system design problems.

The advantages of an analysis method based on coupling FDTD and SPICE are multifold:

- both methods work in the time domain and are therefore suitable for treating nonlinear elements;
- the problem can be conveniently partitioned into full wave and circuit parts;
- the circuit part of the problem is handled by a general, widely used and trusted simulator for which there is an abundance of model libraries for semiconductor elements, logical gates, and integrated circuits;
- adding more ports to the structure does not add significant computational complexity to the problem. This is in contrast to macromodeling approaches where the computational complexity increases in proportion to the number of ports;
- errors and problems associated with frequency domain transformations or inverse transformations are avoided altogether.

Some of these advantages will be illustrated in the examples.

A few approaches for coupling FDTD and a circuit simulator have been proposed in the literature ([4]–[8]). The basic idea of coupling FDTD and lumped element equations was introduced in [4]. In [5] the method was extended to allow the coupling of device ports in FDTD to circuit simulators. This was done by deriving an equivalent circuit for each FDTD–circuit element interface port as seen by the circuit simulator. A similar method is described in [6]. A concrete integration of FDTD with a general semiconductor device and circuit simulator is described in [7]. All of these methods leave some important issues, such as performing the DC solution in the coupled methods, unresolved. In [8] the DC solution problem is addressed by separating the AC and DC parts of the problem and introducing a DC current source element at each FDTD–circuit element port that needs to be pre-computed with a separate SPICE simulation. In this paper we extend and improve the DC solution process to eliminate the separate DC simulation and to make the process simpler, more accurate and more robust. We also introduce an enhancement to FDTD itself to model skin effect in planar conductors efficiently avoiding excessive conductor meshing. The resulting method is applied to a set of sample problems.

2. Theoretical Foundation of FDTD–SPICE
The coupling of FDTD and SPICE is based on an appropriate finite difference formulation of the curl equation

\[ \nabla \times \mathbf{H} = \varepsilon \frac{\partial \mathbf{E}}{\partial t} + \mathbf{J}(\mathbf{E}) \]  

in a subvolume of the FDTD lattice that represents the circuit element (device) port. The current density term \( \mathbf{J}(\mathbf{E}) \) represents the current through the circuit element. A time dependent equivalent circuit model can be obtained from a discretized version of equation (1). The model is illustrated in Figure 1. At each time step the circuit simulator (SPICE) sees this equivalent circuit when looking into the FDTD lattice. Analyzing this equivalent circuit of the FDTD port together with the attached lumped element using SPICE is equivalent to numerically integrating equation (1). From the FDTD point of view, each port where a circuit element is attached is a special volume of space where the
electric field is calculated by SPICE. In order for SPICE to do this, FDTD needs to supply SPICE with the left hand side of (1) at each time step. Implementationwise, this can be done through interprocess communication between FDTD and SPICE programs.

From a circuit analysis point of view, it is very convenient that the equivalent circuit for each FDTD port is completely independent (uncoupled) of the circuits for the remaining ports. The coupling between the FDTD ports is provided through the FDTD field solution only. This means that the circuit analysis part of FDTD–SPICE is very efficient.

2.1 FDTD–SPICE Analysis Overview
The FDTD–SPICE analysis is performed in the following way. First the problem is partitioned into two parts: 1) the distributed part of the analyzed structure that is to be solved using FDTD and 2) the circuit part of the structure that is to be solved using SPICE. The two parts of the problem are connected through a number of FDTD–SPICE ports. At each time step FDTD calculates the elements of the equivalent circuit for the port and passes the information to SPICE. SPICE uses the information to solve equation (1) and returns the calculated voltage to FDTD. FDTD uses the calculated voltage to update the electric field at the port nodes. The procedure is illustrated in Figure 2.

2.2 DC Analysis
The calculation of the DC solution for the analyzed structure requires the calculation of the initial field distribution in the FDTD part of the structure. This calculation is generally much more expensive computationally than calculating the DC solution in SPICE. The problem can be avoided by taking advantage of the linearity of the FDTD portion of the analyzed structure and separating all of the field, voltage, and current variables into DC and AC components. FDTD can then analyze only the AC part of the problem (the part of the problem that we are really interested in) while SPICE has to work with the total parts of voltages and currents. In order to make SPICE use the actual (DC + AC) voltages and currents, we use the following technique. We introduce a special FDTD resistor element in SPICE which behaves as a small resistor during the SPICE DC analysis while it becomes a constant current source for the transient analysis. The element is connected between those terminals of the FDTD–SPICE ports that are connected together by conductors in the FDTD part of the structure. For DC analysis, the resistors model the DC resistance of the conductors in FDTD and enable SPICE to calculate the correct DC currents in the port without performing a separate simulation. During the transient part of the analysis, the special FDTD resistors become constant current sources and feed DC currents to the SPICE circuit that is attached to the FDTD structure at the port. This ensures that SPICE obtains the total DC + AC voltages and currents at the ports. The procedure is more efficient, general, and applicable to a wider variety of SPICE circuits than the technique reported in [8].
Reducing the number of cells or the number of time steps will have the largest impact on the execution time of an FDTD–SPICE simulation.

A standard way of reducing the number of cells in the structure is the use of nonuniform gridding. For many high frequency applications, nonuniform gridding alone does not improve the computational efficiency of FDTD sufficiently. This is specially the case for problems where the skin effect or proximity effects of the conductors have a significant impact on the overall behavior of the analyzed structure. FDTD is not well suited for analyzing skin effect problems since these problems require detailed gridding of the conductors. The problem is exasperated for planar conductors where the thickness of the conductor is much smaller than the conductor width or length. Discretizing the conductors in the thickness direction on complex structures (such as full PCBs) with a fine grid often results in numerical models that are not solvable in a practical amount of time on today’s computers. It is therefore essential to give special treatment to skin effect problems in FDTD.

An accurate and computationally efficient way of dealing with the skin effect problems in planar conductors is to model the surfaces of planar conductors with surface impedance boundary conditions. Surface impedance boundary conditions model the penetration of the fields into the conductor in the thickness direction, while the discretization in the width and length direction of the conductor is done in the usual manner. This way the current distribution along the conductor width and thickness directions is computed correctly and the current distribution in the depth (thickness) direction is taken care of with an analytical model. In this paper we use an approach that is similar to the method described in [9]. A relationship between the electric and magnetic field components on the surface of planar conductors is established in the Laplace domain. This relationship is analytically invertable and leads to a convolution type relationship between the electric and magnetic field components in the time domain. The function inside the convolution integral is a quickly converging series of exponential functions. Therefore, the convolution can be computed recursively, resulting in an efficient implementation in FDTD.

3. Examples

3.1 PCB Ground Bounce

Example 1, shown in Fig. 3, illustrates a simple FDTD–SPICE problem. The example shows a small PCB with one ground plane and one 3.3 V power plane. The ground and power planes are 1.6 mm apart. The dimensions of the board are 50 mm by 50 mm. Sandwiched between the ground and power planes is a signal layer containing a branching signal trace. The first branch is terminated with a 50 Ω load, the second is terminated with a clamping diode and the third ends in a high resistance load representing a driver input. The excitation to the signal trace is provided by a transistor level nonlinear CMOS driver that is driven by a falling trapezoidal input signal with a 1 ns fall time. The driver gets its power supply from the ground and power planes of the board. The DC voltage source is located near the corner of the board, 5 mm from both edges.

The problem is partitioned into two parts. The distributed planar PCB structure is modeled using FDTD and all of the lumped circuit elements are modeled using SPICE. There are six ports connecting the FDTD and SPICE parts of the structure. One port for the DC voltage source, two ports for the driver and three ports for the three signal trace branches. A 10 nF decoupling capacitor is connected to the power leads of the driver. The voltage at the load is shown in Fig. 4 for the case when the decoupling capacitor is connected across the driver’s power supply terminals and for the case when the capacitor is not connected. The voltage across the power supply terminals of the driver is also shown. This is the line oscillating around the 3.3 V DC level representing the ground bounce noise between the power and ground planes.

Figure 3: PCB structure of Example 1 illustrating a simple FDTD–SPICE problem.

3.2 Crosstalk Measurement vs. Simulation

In the second example we evaluate the accuracy of FDTD–SPICE on a simple crosstalk setup. Figure 5 shows two parallel wires in free space above a ground plane. The wires are 4.674 meters long and separated by 20 mm. They are terminated with 50 Ω resistors to the ground plane. One of the wires is excited with a trapezoidal pulse voltage source.

Figure 4: Voltage on the load of Example 1.
Although this appears to be a low speed problem judged by the rise and fall times of the signal, due to the very large length of the lines, this is really a scaled high speed problem. We are interested in the near end crosstalk voltage on the neighboring line. We also analyze the same structure using a quasi-static model consisting of a coupled lossy transmission line together with the connected circuit elements. The results of the two simulations are shown in Figure 6. The measured near end crosstalk for this example is shown in Figure 7 [10]. It is seen that the FDTD–SPICE result is in good agreement with the measurement.

Figure 5: Two coupled lines of Example 2.

Figure 6: Simulated near-end crosstalk voltage of Example 2.

Figure 7: Measured near-end crosstalk voltage of Example 2.

3.3 Frequency Domain Model vs. Direct Time Domain

In the third example we illustrate the difficulties associated with the use of macromodels generated in the frequency domain and used in the time domain. Fig. 8 shows a sample via structure. The via passes through four reference planes that are connected through a nearby ground via. We analyze the structure using two different approaches. In the first approach we treat the structure as a linear two port system and extract the $Y$ parameters of the via using a full wave simulation. Then we create a frequency domain macromodel for the via in the form of a rational function in the frequency variable $f$. For simple two port structures such as this one, creating macromodels is an attractive solution since the same model can be reused many times in different circuit simulations. Finally, we attach a resistive load to the resulting macromodel, excite the model with a trapezoidal voltage source, and simulate the resulting circuit in SPICE. In the second approach we analyze the same structure with the same source and load directly with FDTD–SPICE. The results of the two approaches are compared in Figures 9 and 10.

Figure 8: Via of Example 3: (a) Cross section; (b) top view.

Figure 9 shows a comparison between the magnitudes of the computed $Y_{11}(f)$ parameters used to generate the two port macromodel and the corresponding $Y$ parameter of the macromodel. The macromodel has the form of a rational function in $f$ with a numerator order of 13 and a denominator
order of 14. The coefficients of the numerator and denominator polynomials were generated with the help of using a least squares fit over a frequency band of 15 GHz [11]. The agreement between the original and fitted data is quite good. In the frequency plot of Fig. 9 the scale on the y axis is already significantly magnified. The peaks in the data go well outside of the plot range and there are still no visible differences between the original and fitted data. The differences between the phases of the original and fitted $Y_{11}(f)$ are just as small. The comparison is similar for the other terms in the $Y$ matrix of the two port.

![Comparison of $|Y_{11}(f)|$ computed vs. obtained from The extracted macromodel.](image1)

Figure 9: Comparison of $|Y_{11}(f)|$ computed vs. obtained from The extracted macromodel.

Figure 10 shows the response of the original via structure shown in Fig. 8 and the response of the generated two port macromodel when the input port is excited with a trapezoidal pulse voltage source and the output is terminated with a 40 Ω resistor. The 0 to 100% transition times (rise and fall) of the exciting pulse are 100 ps. It is seen that the propagation time and the leading edge of the output signal are matched well by the macromodel while the differences in the detail of the two waveforms are easily visible. This example shows a problem that is quite common in practical applications where frequency domain generated models are used in the time domain. Even relatively accurate frequency domain models do not necessarily imply time domain models of the same relative accuracy.

The distribution of the z component of the electric field for the via structure of Fig. 8 is shown in Fig. 11. The fields are plotted on a plane parallel to the x-y plane 38 μm below the top signal trace.

### 3.4 Skin Effect in Planar Conductors

In the fourth and final example we illustrate the use of surface impedance boundary conditions in FDTD–SPICE. Figure 12 shows a small microstrip structure with significant conductor losses. The characteristic impedance of the microstrip is approximately 50 Ω. The structure is terminated with a 50 Ω resistor at the far end and it is excited with a step input voltage whose 0 to 100% rise time is 30 ps. We analyze the response of the line using three techniques. In the first approach we analyze the line using FDTD–SPICE and model the skin effect in the usual way, discretizing the lossy conductors in the thickness direction using FDTD cells. In the second approach we also use FDTD–SPICE but this time we discretize the conductor with just one cell in the thickness direction. We also model all the conductor surfaces with surface impedance boundary conditions. In the third approach we treat the microstrip as a lossy transmission line with frequency dependent conductor losses and calculate the time domain solution using an inverse discrete Fourier transform. The responses obtained using the three techniques are shown in Fig. 13.

![Input voltage pulse Direct FDTD-SPICE SPICE Macromodel](image2)

Figure 10: Via response calculated using two approaches

![Field distribution on the structure of Example 3.](image3)

Figure 11: Field distribution on the structure of Example 3.

It is seen that all three techniques agree reasonably well for this problem, validating both FDTD–SPICE approaches. In practical applications the model could easily become more complicated. For example the microstrip trace could have a few bends, meanders, or impedance matching elements in it. These complications in the distributed part of the analyzed structure would quickly complicate the quasi-TEM approach (at high frequencies), yet they pose no additional problems to FDTD–SPICE.
5. Concluding Remarks

In this paper we have described a hybrid full wave–circuit simulation method based on FDTD–SPICE and applied the method to a few example structures. The method ties together two general, well proven, time domain simulation methods. In this paper we focused on simple examples which can easily be reproduced, but which still illustrate the potential of the method. With the continuing rapid advances of desktop computers the method is becoming practical for a growing set of real-world problems. As in the case of FDTD, it can be expected that the method will rapidly gain in popularity in the next decade.

References