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Full Wave Signal and Power Integrity Analysis of Printed Circuit Boards Using 2D and 3D FDTD–SPICE Methods

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Abstract
Two closely related time domain methods for analyzing PCBs with full wave accuracy are introduced. The methods are based on a technique that couples the full wave FDTD method with the circuit simulation approach of SPICE. The problem under consideration is divided into distributed and circuit parts that are solved together using FDTD–SPICE techniques. In one method, the distributed part of the structure is treated as a 3D problem and in the other as a 2D problem. The methods are evaluated through a design case study. Tradeoffs in the accuracy and computational performance are considered. Results obtained with the widely accepted FDTD method are used as a reference.

Author Biography
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Norio Matsui holds a Ph. D. from Waseda University, Tokyo and was a researcher in NTT Labs for over 16 years. During this period he developed noise simulation tools for Signal and Power Integrity as well as physical designs for high speed tele-switching systems. Apart from authoring numerous papers, he also lectured at Chiba University. He is currently President of Applied Simulation Technology and is actively involved in Power Integrity, Signal Integrity, and EMI/EMC solutions.
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1. Introduction
The ever increasing data rates in modern digital circuits, as well as the higher operating frequencies and larger bandwidths of RF circuits, place new demands on circuit and system designers. This is especially true in the design of printed circuit boards (PCBs). Due to the relatively large electrical dimensions of today’s PCBs, interconnect structures play an important role in the performance of the circuit. Typical interconnect design problems in high speed digital PCBs are the determination of optimal component placement based on electrical and thermal considerations, design of the power distribution system based on the specified power integrity (PI) requirements, and routing of signal connections to satisfy signal integrity (SI) requirements. In addition, the radiated electric and magnetic fields, that are the cause of electromagnetic interference (EMI), must be kept within the required limits. These tasks and effects are tightly coupled. Accurate analysis of PI, SI, and EMI effects is critical for efficient system design.

Accurate analysis of power and signal interconnects on today’s PCBs is a problem that requires significant computational effort. Due to the complex geometries and high operating frequencies, conventional quasi-static analysis is often not sufficient and full wave analysis is required. The large number of interconnects on the PCB together with the small feature size accentuate the problem. The presence of nonlinear devices restricts the computational techniques that can be used.

In the process of choosing an analysis method for leading edge PCBs, we should consider the following. Most of the devices on the PCB are on integrated circuits (ICs) and are small compared to the wavelength propagating at the highest frequency of interest. Therefore, the devices lend themselves to circuit modeling. These devices can be nonlinear, requiring that the simulation be performed in the time domain. Power and ground connections of the devices as well as coupling between nearby devices need to be modeled. All of these requirements point towards a SPICE based circuit analysis approach for the devices.

In contrast to the devices, the on board interconnects (and sometimes the package interconnects) have considerable electrical lengths at the highest frequency of interest. Also, their geometry can be complex resulting in propagation that cannot be described accurately by quasi-TEM models. Their analysis, in general, requires full wave methods. Candidates for the full wave analysis are frequency domain and time domain methods. Frequency domain methods are well adapted for the analysis of passive linear interconnect structures. They can also be used to extract frequency domain macromodels of the interconnect. If these frequency domain macromodels are inverse transformed back to the time domain, they can be used together with the device models in a SPICE based circuit solution. The same macromodel can be used again and again in multiple simulations improving the efficiency of repeated analysis. However, the problems of model order reduction or inverse transforms are not trivial. The associated techniques are computationally complex and burdened with problems in the algorithm robustness and accuracy. A more straightforward approach is to use time domain full wave methods to solve the problem directly. A logical candidate here is the finite difference time domain (FDTD) method. This leads us to FDTD–SPICE techniques.
2. FDTD-SPICE Overview

FDTD–SPICE techniques are based on the following approach [1–5].
The problem is partitioned into two parts. The first part is the nonlinear circuit part that is solved using SPICE and the second part is the linear distributed part that is solved using FDTD. Ports that connect the SPICE partition to the FDTD partition are chosen. The two methods are coupled through ports and exchange port voltage and current information at each time step. The procedure is illustrated in Fig. 1.

For computational efficiency reasons, the solution is separated into DC and AC components. The DC solution is calculated only in SPICE by connecting DC resistors between the ports which are connected by conductors in the FDTD structure. After the SPICE DC solution is found, FDTD works only with the AC part of the solution. This separation of the solution into DC and AC components can be done due to the linearity of the full wave part of the structure as long as SPICE works with the total solution (DC + AC). Since FDTD works only with AC components, a static field solution (DC) is never required. Also, FDTD gives us only the interesting part of the field solution – the time-varying part. The procedure results in both the conventional SPICE voltages and currents in the analyzed circuit and the field solution in the full wave part of the structure.

![Figure 1: Illustration and equivalent circuit of the FDTD–SPICE approach:](image)

(a) FDTD–SPICE port model in FDTD and in SPICE;
(b) FDTD–SPICE interface.

In terms of the overall computational cost, the most expensive part of the calculation procedure is in solving the FDTD part of the structure. This is because of the large number of cells that are required to model general 3D interconnect structures. Therefore, most of the effort in improving computational efficiency should be directed towards reducing the FDTD solution time. A good way to do this is to analyze a larger portion of the structure under consideration in SPICE and a smaller portion in FDTD.

The partitioning between the circuit and full wave parts can be accomplished in many different ways. Different partitioning approaches result in different FDTD–SPICE methods. For example, the distributed part can be modeled as a 3D problem or a 2D problem with corresponding differences in the coupling mechanism between the full wave and circuit partitions. Two such methods are described on a design case study in the following section.
3. Design Case Study: Small high speed printed circuit board

The design under consideration consists of a small high-speed printed circuit board with two dual inline package (DIP) components on the top side (Fig. 2). The board has four conductor layers. The top and bottom conductor layers are used for signal routing. The routing on the top signal layer is performed in the horizontal direction and the routing on the bottom layer is in the vertical direction. The higher of the two middle layers is the power plane and the lower is the ground or reference plane. A 3.3 V DC voltage source is connected between the power and reference planes at the lower left corner of the board, 15 mm from both edges. The top left pin of each IC is the Vcc pin and it is connected to the power plane through a power via. The bottom right pin of each IC is the ground pin connected to the reference plane through a ground via. The chosen driver pin is the top right pin of the top left IC. A high resistance load is connected between the bottom left pin and the ground of the lower right IC. A signal trace routed both on the top and bottom signal layers connects the driver and receiver. The signal connection passes through two signal vias.

Figure 2: Small high speed PCB with four conductor layers: (a) top view, (b) front view.
A small and simple board was chosen for two reasons: 1) computational efficiency, 2) easier understanding and visualization of the dominating effects. We ensure that all of the important large board SI and PI effects are present on this small board by using fast excitations. By using a simple board we have the luxury of analyzing the full board including the IC packages using FDTD for reference and comparison purposes. Although the board is relatively simple, it is representative of the type of analysis problems PCB designers are faced with today.

Our main interest is in the interconnect part of the board. This part consists of the IC packages, signal traces, vias, power and reference planes. We characterize this part first. Nonlinear devices complicate the response and often mask the relevant effects. In this work we introduce nonlinearities last, once the interconnect part of the problem is understood.

### 3.1 FDTD Characterization of the Linear Problem

In order to characterized the linear part of the structure we have too look inside the package. Figure 3 shows a simplified view of the package and its connection to the surrounding interconnects. The driver is connected to the power and reference planes through pins 1 and 14, respectively. Therefore, to characterize the linear part of the structure that the driver sees we at least need to characterize the interconnect at two ports, A and B.

![Figure 3: Simplified view of the interconnect structure around the driver and the excitations.](image)

We characterize the structure by applying a current excitation at each port separately and by calculating the short circuit response of the interconnect. The current source waveform has the shape of a unit step function with a 30 ps ramp-shaped rising edge. The amplitude of the current pulse is 33.33 mA. The width of the pins in Fig. 3 is 2 mm, their thickness is 0.5 mm, their separation in the direction of current source A is 9 mm and in the direction of current source B is 34 mm. The separation between adjacent pins (shown in Fig. 2) is 1 mm. A short circuit load is contained in the second IC.

Due to the differences in the interconnect geometries between the power and ground pins (different current paths) and their corresponding supply plane connections, we can expect different responses for excitations A and B. The interconnect responses for cases A and B at the signal trace input are shown in Fig. 4. The corresponding responses at the receiver end of the signal trace are shown in Fig. 5. The voltages in this figure are defined in terms of the line integral of the electric field from a center point on the signal trace to the closest point on the ground plane below it. It is seen that the excitation connected between the power and output pins of the driver produces a faster response. It should also be noted that the high frequency details of the waveforms are considerably different between cases A and B, indicating that the higher frequency components are very sensitive to the current path for this high-speed excitation.
In order to understand the nature of the waveform differences better, we look at the voltage distributions in the structure (case A). Figure 6 shows the spatial distribution of the voltage between the top signal layer and the power plane directly below it. The voltage for each (x, y) point on the plot is defined in terms of the line integral of the electric field between the power and signal layers for the given (x, y) coordinates. We can see the leading edge of the propagating wave as it passes through the package and reaches the first signal via. The propagating wave then changes layers and after propagating on the
bottom layer finally reaches the receiver. Coupling noise within the package is visible. We can also see
the effect of signal reflection and leading edge degradation from the two vias.

Figure 6: Spatial distribution of the voltage between the top signal and power layers at t=200 ps.

The field behavior between the power and ground planes of case A after the wave reaches the first signal
via is shown in Fig. 7. From the figure we can see that once the propagated signal reaches the signal via,
parallel plate mode waves are excited between the power and reference planes. These waves propagate
radially from the via until they reach the board edges. After this, a combination of standing wave modes
is established between the planes. The voltage between the power and ground planes will play a part in
our voltage waveforms of Figs. 4 and 5, contributing to the high-frequency ripples. This is because the
integration path that defines the voltage passes between these planes.

Figure 7: Voltage distribution between the ground and power planes for case A at t=400 ps
showing the parallel plate modes excited by the first signal via.
The corresponding voltage distribution for case B is shown in Fig. 8(b). It is seen that the waves between the power and reference planes are first excited at the ground via of the driver IC. Since the ground via ends inside the power–ground structure (blind via), the resulting currents are confined between the planes and the waves have a higher amplitude than in case A. The result of the stronger parallel plate disturbance is also visible in the voltage waveforms of Figs. 4 and 5.

![Figure 8: Voltage distribution the ground and power planes for case B: (a) t=200 ps, (b) t=400 ps.](image)

The magnitude of the total current in the power plane for the excitations of case A and B are shown in Fig. 9. It is seen that the current of case A is concentrated mostly under the signal trace and under the excitation with very little spreading around the board. In case B the current is spread around the ground via. This is consistent with the voltage waveforms of Fig. 8.
Figure 9: Current distribution on the power plane for excitations of cases A and B, respectively.

In the FDTD characterization we analyzed the interconnect structure associated with our signal net by leaving out the nonlinear IC components. The accuracy so far is limited by the spatial resolution of the FDTD grid in the x, y, and z directions. It is also determined by the geometrical detail of the exciting current source models (3D volume regions). The computational cost of the analysis is determined mainly by the grid. Our next step is to reduce the computational cost and to allow the inclusion of arbitrary circuits at the IC pins. To achieve this we employ FDTD–SPICE.

3.2 3D FDTD–SPICE Model

FDTD–SPICE techniques can be applied to the problem of Fig. 2 in several ways. One approach is to model the circuits connected between the pins in SPICE and to model the rest of the structure in FDTD exactly as we did above. Although this is the most accurate approach, it does not have any performance benefits and it is limited to relatively simple boards. A significant portion of computational effort in the
above FDTD model was spent on the analysis of the components on the board together with their packages. The components had to be discretized and this required a significant number of FDTD cells. The computational cost can be lowered by modeling more of the fine features of the structure in SPICE. By modeling the components in SPICE, the FDTD grid will require significantly fewer cells in the z direction (height). In this section we investigate such an approach. Simple lumped circuit package models are used to evaluate the lower limit of the obtainable accuracy.

For purposes of circuit modeling with SPICE, we can extract the excess package inductance and capacitance using a static field solver, frequency domain quasi-dynamic solver, or a full wave solver. In this work we used a static field solver to calculate the capacitance of the pins and a frequency domain quasi-dynamic field solver to extract the partial inductance at two frequencies. From this capacitance and partial inductance we subtract the capacitance and partial inductance of the the FDTD–SPICE ports used in the FDTD grid. We still use our current source excitation for comparison purposes. The resulting driver model is shown in Fig. 10. A similar lumped model is used for the load with the current source replaced by a short circuit.

![Figure 10: SPICE portion of the circuit for the linear driver of Fig. 3.](image)

The resulting voltage responses at the driver and receiver ends of the signal trace are shown in Fig. 11 together with the reference FDTD responses. It is seen that the important effects are captured by the simplified package model. There are differences in the high frequency components, as can be expected from previous analyses. The obtained grid simplification speeds up the analysis by a factor of 2.8.

It is important to note that most of the differences between the 3D FDTD–SPICE results and the reference FDTD results are due to the simple package and pin model of Fig. 10. It is possible to synthesize more complex circuit models for the IC package that will give better accuracy, but we will not explore the topic of package modeling further in this paper.
Figure 11: 3D FDTD–SPICE computed driver end voltage waveforms for the two excitations of Fig. 3: FDTD Case A (solid), FDTD Case B (dashed), 3D FDTD–SPICE Case A (dotted).

Figure 12: FDTD–SPICE computed receiver end voltage waveforms for the two excitations of Fig. 3: FDTD Case A (solid), FDTD Case B (dashed), 3D FDTD–SPICE Case A (dotted).
3.3 2D FDTD–SPICE Model

The speedup obtained in the previous section is useful but not sufficient for the analysis of the most complex boards on today’s computers. Additional performance improvements can be obtained by modeling the all of the signal traces using transmission line models in SPICE. These transmission line models are connected to the planes at the vias. The vias are also modeled using equivalent circuits. The only part of the structure that remains to be modeled in FDTD are the power and ground planes. Figure 13 illustrates the resulting 2D FDTD–SPICE model.

![Figure 13. 2D FDTD–SPICE model of the board.](image)

The voltage response of the above model at the receiver end of the signal trace is shown in Fig. 14 together with the corresponding FDTD and 3D FDTD–SPICE models.

![Figure 14: 2D FDTD–SPICE response at the receiver end of the signal trace.](image)
It is interesting to note that the 2D FDTD–SPICE of this structure gives an accuracy comparable to the 3D FDTD–SPICE approach with the crude package model of Fig. 10. The speedup obtained for this simple layer stackup is an additional factor of 2.33 over the simple 3D FDTD–SPICE model corresponding to Fig. 10.

The above 2D FDTD–SPICE approach models all of the small details of the structure using SPICE, yet it still takes into account the most significant effects occurring between the power and ground planes of the structure by discretizing the planes using a 2D grid. The most important restrictions of the 2D FDTD–SPICE approach are that the top-most and bottom-most planes in the layer stackup must be mostly solid to confine the fields between the planes. If significant voids in the planes exist, 3D analysis methods should be used.

### 3.3 Nonlinear Driver

Now that the responses of the above models are examined and compared, we are ready to introduce nonlinearities into the analyzed structure. A CMOS driver is attached to the first package. The complementary MOS transistors have a gate length of 0.1 µm and a width of 0.5 µm. The driver is driven with an input signal of rise time of 30 ps. The response at the receiver end of the signal trace is shown in Fig. 15. The figure shows the response of our board obtained using 3D FDTD–SPICE together with the response obtained from conventional transmission line signal integrity analysis. In the transmission line model, the ground and power planes are assumed to be short circuited near the vias and the vias are modeled using lumped LC models. The same CMOS driver is driving the line in both cases but an ideal DC voltage source is connected between the power and ground terminals of the driver in the transmission line model. The FDTD–SPICE approach models only the driver and receiver in SPICE. The rest of the structure is modeled using FDTD. Large differences between the two results are visible. The differences are mainly caused by the lack of power and ground current path modeling in the second approach. As seen in the previous characterization, ground current paths introduce considerable parasitic effects for this signal resulting in a significant slowdown of the edges.

![Figure 15: 3D FDTD–SPICE response of CMOS driven structure compared with transmission line model without ground and power supply current path modeling](image)
4 Concluding Remarks

Two FDTD–SPICE techniques were introduced in this paper and demonstrated on a small printed circuit board. The first technique models the components in SPICE using circuit models and models the board in FDTD using a 3D grid. The second method models everything but the power and reference planes in SPICE and uses a 2D model for the analysis of the reference planes. For linear elements, the obtained results were compared to the reference result obtained using the FDTD method. The 2D model introduces significant performance benefits in the analysis while still capturing the dominant PI and SI effects on this board.

The advantages of FDTD–SPICE methods are multifold:

- both methods work in the time domain and therefore are suitable for handling nonlinear elements;
- the problem can be flexibly partitioned into full wave and circuit parts using numerous approaches;
- the circuit part of the problem is handled by a general, widely used simulator for which there are many available model libraries;
- adding more ports to the structure does not add significant computational complexity to the problem. This is in contrast to macromodeling approaches where the computational complexity increases in proportion to the number of ports;
- errors and problems associated with frequency domain transforms or inverse transforms are avoided.

References