SI and EMI Analysis of Analog Circuit Board
Combination of PEEC and MOR

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Abstract
A method for analyzing SI and EMI of analog circuit board considering the effect of analog patterns has been proposed. This method uses the combination of PEEC (Partial Element Equivalent Circuit) and MOR (Model Order Reduction). Major contributors to signal, power and EMI noise in high power supply circuits are the parasitics of arbitrary shape conductor patterns between discrete components such as power MOS transistors and passive components. The conductor patterns are modeled as meshed RLGC network circuits, and then compressed into a compact circuit model. Voltage and current waveforms in time domain and EMI in frequency domain are simulated by using the obtained macro model and nonlinear devices.

Keywords
SI, EMI, PEEC, MOR, Switching Power Supply, SPICE, Simulation, Analysis, Macro Modeling.

INTRODUCTION
Most of conventional EMI analyses have been focusing on high speed digital circuit boards. Conventional analysis of analog circuits such as switching power supply or operational amplifier circuits has been ignoring the effect of conductor layout patterns of a printed circuit board on waveforms. Today's power supply circuits used for driving motors of automobiles still are operated at much lower frequency than digital circuits. However, they consume more and more power than ever. In addition, it is very normal that such analog circuit boards shown in Fig.1 have no solid ground and power planes to cut cost. Therefore, AM and LF noise generated by analog circuit boards has become very serious issue for AM radio and CAN (Controller Area Network) bus. Major contributors to the noise are the inductance and capacitance of layout conductor patterns between discrete components. In order to predict the low frequency noise waveforms and resultant EMI noise for the high power analog circuit boards, the combination of PEEC [1] model and MOR has been proposed. CAD data for analog patterns can automatically be converted into PEEC model by geometry calculation for arbitrary shapes and manual drawing methods. Since the analog patterns span an entire board, the model becomes very huge. Therefore, the generated PEEC model must be compressed into smaller size model by MOR.

There are many methods to compress large circuits. One of the methods is to extract N-port parameters first using the circuit extracted from the PEEC model. The extracted N-port parameters are converted into SPICE readable model in time domain. This can be performed by fitting the rational function expansion or frequency table model [2]. Since the size of the PEEC model considering coupling between isolated analog pattern islands becomes huge, an efficient circuit solver has been developed [3]. The other method is to directly compress a large circuit to small one without extracting N-port parameters [4]. A key to realize this method is to provide a stable model. Since power circuits use large time constant devices such as choke coils and capacitors with nonlinear devices in time domain, the introduction of interconnection models makes time domain analysis so sensitive and results in no convergence. In order to improve convergence, a new method of controlling frequency range has been developed.

Figure 1. Analog Patterns of Analog Circuit Board.
Meshing for PEEC Model

High speed digital circuit boards use impedance controlled patterns for signal traces. The shape of such patterns is rectangular and it can be drawn by auto router. This is called as digital pattern. On the contrary, most of patterns between power discrete devices are drawn by hand. The shapes of the analog patterns are arbitrary such as polygon, arc, and round. Therefore, usual transmission line model can not be applied to the analog patterns. Figure 2 shows various meshing for the analog patterns.

(a) No meshing:
This is normally used for SI analysis of digital circuits. The shape of signal traces is rectangular. Arbitrary shape power and ground patterns are simply assumed to be solid planes ignoring vias, holes and slits of the arbitrary shapes. Therefore, signal traces can be modeled as transmission lines assuming (quasi-) TEM.

(b) Triangle meshing:
This provides best fitting to arbitrary shape. However, triangle mesh is not widely used for PEEC. Because it may not be easy to get equivalent circuit PEEC model. Coupling model between cells and strip may lose accuracy.

(c) 90 degrees meshing for all patterns:
Coupling for all xyz directions can be accurately considered. However, very fine meshing may be needed for narrow strip patterns or very closely located patterns.

(d) 90 degrees meshing only for large patterns:
Since narrow strips are not meshed, coarse meshing can be used. This is most practical for real board applications. Ignoring coupling between cells and strip may lose accuracy.

The last two methods can use adaptive (irregular) meshing. If method (c) or (d) is applied to arbitrary shapes, then PEEC model is created by a program. All mesh cells can be described in coupled or uncoupled RLGC equivalent circuit.

N-port Extraction and Conversion to Compact Model

A large size circuit can be compressed by converting a circuit model into N-port parameters which have less number of nodes. This is so called Model Order Reduction (MOR). However, this method has a problem when applying to a huge whole board PEEC model. With an increase in the number of the nodes of the final circuit model, it takes long time to extract N-port parameters by conventional circuit simulator such as SPICE. To resolve this issue, we have developed a super linear solver (SLS). It can use memory effectively and drastically speed up the simulation. SLS consists of parser and solver. Once we get N-port parameters, we must convert them into SPICE readable elements in frequency and time domains. This can be performed by fitting the rational function expansion shown in Fig. 3 or frequency table model shown in Fig. 4. Circuit simulator uses state variable approach and IFFT + convolution for the rational function expansions and frequency table model, respectively.

Figure 2. Meshing for PEEC Model

Figure 3. Fitting of Rational function.
Electrically short structures should use rational function approximation. This enables us a fast transient simulation. Electrically long structures should use frequency tables. This is slower than rational function, but no need for frequency fitting. Figure 5 shows an example of the rational function for electrically short structure. Figure 6 compares the rational function and the frequency tables for electrically long structure.

### Direct Conversion to Compact Model

In order to improve the convergence in applying the converted compact model to time domain simulation with nonlinear devices and very long time constant devices, we have added user controllable frequency range to previous algorithm [4]. Figure 7 shows examples for a lumped circuit model with user specified maximum frequency (minimum time). Below the frequency, Y-parameter shows good tracing. Figure 8 compares the time domain simulation for the corresponding models. Even if the Y-parameter does not fit beyond the specified upper frequency, the waveforms of compressed model show good agreement with those of uncompressed model. Direct Model also uses SLS.

### Figure 4. Frequency Table.

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Real</th>
<th>Imag</th>
</tr>
</thead>
<tbody>
<tr>
<td>f1</td>
<td>P(f1)_r</td>
<td>P(f1)_i</td>
</tr>
<tr>
<td>f2</td>
<td>P(f2)_r</td>
<td>P(f2)_i</td>
</tr>
</tbody>
</table>

### Figure 5. Fitting in the rational function for electrically short structure.

![Figure 5. Fitting in the rational function for electrically short structure.](image1.png)

### Figure 6. Rational function (upper) and frequency table (lower) for electrically long structure.

![Figure 6. Rational function (upper) and frequency table (lower) for electrically long structure.](image2.png)

### Figure 7. Direct Conversion for two minimum times (upper: 500ps, lower: 100ps).

![Figure 7. Direct Conversion for two minimum times (upper: 500ps, lower: 100ps).](image3.png)

### Figure 8. Time Domain Analysis using Direct Conversion Model. (Upper: Original, Middle: 500ps Lower: 100ps)

![Figure 8. Time Domain Analysis using Direct Conversion Model. (Upper: Original, Middle: 500ps Lower: 100ps).](image4.png)
ANALYSIS OF Switching Power Supply
We applied our method to a switching power supply whose power circuit other than control circuits is shown in Fig. 9. The switching frequency is 20 KHz. There are four power MOS transistors. Pair of cables connects output terminals of the circuit board to a motor. Figure 10 shows a top view of the printed circuit board with four layers. Discrete power components are interconnected by arbitrary shape patterns.

Figure 9. Magnetic Probe and Test Board.

Figure 10. Switching Power Supply Board.

Figure 11 is a typical procedure of SI and EMI simulation. A mesh generator makes meshes for the specified nets with arbitrary shape patterns of CAD. All mesh cells are modeled as RLGC lumped or distributed model calculated with field solver. The mesh patterns shown in Fig. 12 are converted into a compact model either by N-port parameter extraction plus SPICE readable model for rational function model or frequency table, or by direct conversion. Obtained compact model with nonlinear device models can be solved by circuit simulator or EMI simulator.

Figure 11. Simulation Flow.

Figure 12. Mesh Patterns.
Results of Simulation
Figure 13 compares the voltage waveforms at loading points for a motor. Directly connected device model with no patterns has no ringing. Figure 13 (b) indicates the effect of patterns on the waveforms.

Figure 13. Effect of patterns on voltage waveforms at loading points for a motor.

Figure 14 compares Y-parameters of two patterns between devices between the original PEEC model and its direct conversion model. Both curves match pretty well.

Figure 14. Comparison of Y-Parameters between the original PEEC model and the directly converted compact model.

Figure 15 compares voltage waveforms at the loading points for corresponding models. Both waveforms are almost the same.

Figure 15. Comparison of waveforms at loading points between the original PEEC model and the directly converted model.

Figure 16 shows CPU time to simulate the power supply circuit considering patterns for the original PEEC model with no MOR, MOR by N-port parameter fitting, and MOR by direct conversion. The number of circuit elements is 9,000. The number of nodes is 45.
EMI Analysis

Since the discrete components mounted on a switching power supply board are tall and complex, we may estimate the radiation noise from the patterns between them.

Once current distributions are calculated by the previously mentioned methods, radiation noise can be evaluated for given conditions of EMC site even at very low frequencies [5-6]. Figure 17 is an example of the radiation noise at 3 meter from the switching power supply board under 500KHz. The upper radiation can be reduced by low impedance of patterns. Decrease in inductance and increase in capacitance can reduce the EMI noise. Radiation along cables to motors from switching power supply board can also be evaluated.

CONCLUSION

A new method for analyzing SI and EMI for analog circuit boards with arbitrary shape patterns between discrete components has been proposed. The model uses PEEC described in RLGC elements of mesh patterns. Since such a model becomes huge, MOR is introduced. The first method is to extract N-port parameters of the PEEC model and to convert into compact circuit model. This can treat frequency dependent elements. However, this method may meet a difficulty in fitting rational function or a problem of convergence in IFFT in circuit simulator. The second method can be applied to PEEC model described in frequency independent elements. The advantage of our method for this is to control maximum frequency to improve convergence. We have also introduced SLS for fast circuit simulation for huge circuits. Our method can also be applied to digital and mixed mode circuit boards with arbitrary shape power and ground patterns.

REFERENCES