PRESS RELEASE

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Applied Simulation Technology
6475 Camden Ave. Suite 102A
San Jose, CA 95120
Tel: (408) 436-9070
Fax: (408) 436-9078

Parallelization of FDTD-SPICE with Port Subdivision

San Jose, California-September 20, 2017. Applied Simulation Technology has successfully implemented parallelization of FDTD (3d Finite Difference Time Domain Electromagnetic Field Solver) and SPICE (industry standard simulation program for ICs) using unique techniques that allow domain port subdivision.

The finite difference time-domain method (FDTD) is a general full-wave analysis technique for solving a wide range of three dimensional electromagnetic problems encountered in electronic design. Nonlinear circuit elements may be included in the simulation by interfacing FDTD with a general purpose circuit simulator such as SPICE. The resulting hybrid field-circuit simulation method, also known as FDTD-SPICE, is more general than harmonic balance methods but is limited by its large memory requirements and long computation times.

Parallelizing FDTD-SPICE reduces the computation time and gives the method the potential to be applied to complex real-world problems. Previous version of ApsimFDTD was parallelized. But ApsimFDTD-SPICE was not parallelized. In order to parallelize ApsimFDTD-SPICE, we have proposed a new method to subdivide both the FDTD structure and the FDTD-SPICE ports. This approach realized generalization of the method of parallelizing FDTD-SPICE that subdivides the FDTD structure, as well as the FDTD-SPICE ports, into subdomains. Each computational subdomain is assigned to its own parallel processing computers.

FDTD-SPICE ports are the regions of the FDTD grid that are used as interfaces between the field (FDTD) and the circuit (SPICE) parts of the simulation. Since they may be positioned anywhere in the FDTD structure, their subdivision and inclusion in the parallelization scheme is a key part of the overall procedure.

During the simulation, neighboring FDTD subdomains exchange field component information between each other while the FDTD-SPICE ports exchange the port voltage and current information between FDTD and SPICE. SPICE sees the subdivided FDTD-SPICE ports as equivalent circuits whose element values are calculated by FDTD. Each FDTD-SPICE port subdomain contributes to its calculated element values though

calculations performed within its domain. The results are then assembled and communicated to SPICE at each time step. ApsimP_FDTD-SPICE uses special techniques to quickly get DC solution already developed for ApsimFDTD_SPICE. The parallelization scheme allows for larger real world problems to be analyzed in a more timely fashion since it takes advantage of multiple CPU cores.

For more info contact:

Fred Balistreri
Applied Simulation Technology
6475 Camden Ave. Suite 102A
San Jose, CA 95120
408-436-9070 ext. 102
email: fred@apsimtech.com
web: www.apsimtech.com